4. (NEW) The multiplex conversion unit according to claim 2, wherein said multiplex conversion unit is applicable to one of 4-fiber Bi-directional Line Switched Ring (BLSR), 2-fiber BLSR and Linear ADM (LADM) networks by selectively combining said four types of circuit packs.

REMARKS

Claims 1-2 are pending. By this Amendment new claims 3 and 4 have been added.

The Office Action rejects claims 1-2 under 35 U.S.C. § 102(e) over Ball (U.S.P. 5,583,855). This rejection is respectfully traversed.

In the Ball apparatus, the TSI (Time Slot Interchange) unit and the TSA (Time Slot Assignment) unit are always used in combination. In order to increase low-speed interfaces at a node in the Ball system, low-speed lines are increased by the parallel connection of the TSI units. In contrast, Applicants claimed invention differs therefrom. In particular, in configuring a node requiring only the TSA function, Applicants invention uses the connecting circuit pack as recited in claims 1 and 2 in order to connect the high-speed interface circuit pack and the low-speed interface circuit pack. On the other hand, if the TSI function is required, Applicants invention uses the add/drop circuit pack in place of the connecting circuit pack.

Usually, the high-speed interface circuit pack, the low-speed interface circuit pack, the TSA circuit pack for realizing the TSA function, and the TSI circuit pack for realizing the TSI function, are designed separately. For example, the TSA circuit pack is used to realize the UPSR (Uni-directional Path Switched Ring). If a higher performance function is required, the node is configured by replacing the TSA circuit pack by the TSI circuit pack.

To reduce the manufacturing costs for a node, it is advantageous to reduce the number of circuit packs and the cost of a circuit pack itself. To attain the total cost reduction of nodes, the Applicants invention employs, to realize the UPSR, such a system that the function of the TSA circuit pack is included in the high-speed interface circuit, while the low-speed interface circuit pack and the high-speed interface circuit pack are connected with a low-cost connection circuit pack.

If the UPSR alone were realized, a connection circuit pack would be unnecessary, because a node would be realized by merely connecting the high-speed interface circuit pack and the low-speed interface circuit pack directly. In the Applicants invention, however the connecting circuit pack is used on purpose to also realize the TSI function easily by detaching the connecting circuit pack and attaching the add/drop circuit pack having the TSI function in place of the connecting circuit pack.

In contrast, Ball's apparatus fails to disclose or suggest the Applicants configuration allowing function addition by exchanging a circuit pack having the TSI function as set forth above. Ball's apparatus also fails to disclose or suggest detaching the TSI circuit pack to reduce the cost of a node in case that the TSI function is unnecessary. Accordingly, Ball does not anticipate claims 1 or 2 of the present application and Applicants request withdrawal of the rejection.

The Office Action rejects claims 1-2 under 35 U.S.C. § 102 over Furuta (USP 5,600,648). This rejection is respectfully traversed. Furuta is directed to monitoring specific bytes in the SDH signal. Fig. 19 of Furuta apparently shows the configuration of a conventional SDH node. A demapping unit/mapping unit as shown in Fig. 19 of Furuta does not include a circuit pack together with interfaces, the line selection unit being realized by a low-cost connecting circuit pack, and in the case of the TSI function, the connecting circuit pack being replaced by the add/drop circuit pack as required by the claims of the present application. Accordingly, Fig. 19 of Furuta is quite different from Applicants claims invention and it is not anticipated thereby. Accordingly, Applicants request withdrawal of the rejection of the claims over Furuta.

The Office Action rejects claims 1-2 under 35 U.S.C. § 102 over Hurlocker (USP 5,490,142). This rejection is respectfully traversed.

Hurlocker shows a cross-connect as shown in Fig. 3 which differs from Applicants connecting circuit pack, because the Hurlocker's cross-connect necessitates some active components to realize the cross-connect function. In Applicants claimed invention, the cross-connect function is unnecessary in a case where the TSI function alone is needed. The TSA function is included in the high-speed interface circuit pack, and the high-speed interface

circuit pack and the low-speed interface circuit pack are connected by the connecting circuit pack on which no active components are mounted so as to reduce the cost of the node. If the TSI function is required in Applicants claimed invention, the connecting circuit pack is replaced by the add/drop circuit pack. Because Hurlocker does not show these features, Hurlocker does not anticipate the claims of the application and Applicants request withdrawal of the rejection.

The Office Action rejects claims 1-2 under 35 U.S.C. § 103 over Yamamoto (USP 5,546,403). This rejection is respectfully traversed.

Figs. 4 and 7 of Yamamoto show block diagrams constituting a node. Applicants claimed invention reduces manufacturing costs of the entire node by replacing the circuit pack having the TSI function by the low-cost connecting circuit pack on which no active components are mounted in the case where the TSI function is unnecessary. Yamamoto does not include these features and accordingly does not anticipate the claims of the application. Applicants request withdrawal of the rejection.

The Office Action rejects claims 1-2 under 35 U.S.C. § 102 over Shioda (USP 5,537,393). This rejection is respectfully traversed.

Shioda shows in Figs. 5 and 7 block diagrams constituting a node. Shioda's TSA/TSI unit in the figures realizes both the TSA and TSI functions. In contrast, in Applicants claimed invention, if the TSI function is not required, the circuit pack having the TSI function is replaced by the low-cost connecting circuit pack to reduce the manufacturing costs of the entire node. Because these features are not shown in Shioda, Shioda does not anticipate claims of the application and Applicants request withdrawal of the rejection.

The Office Action rejects claims 1-2 under 35 U.S.C. § 103 over Lee (USP 5,799,001). This rejection is respectfully traversed.

Lee includes the HVC connection matrix, the add/drop multiplex circuit pack and the like which are indispensable to a node. However, Lee fails to disclose or suggest Applicants claimed feature mentioned above in which, if the TSI function is not required, the circuit pack having the TSI function is replaced by the low-cost connecting circuit pack to reduce the

manufacturing costs of the entire node. Because Lee fails to disclose this feature, Lee does not anticipate claims of the application and Applicants request withdrawal of the rejection.

The Office Action rejects claims 1-2 under 35 U.S.C. § 102 over Hiramoto (USP 5,471,476). This rejection is respectfully traversed.

Applicants claimed invention may be utilized to realize the ADM function as shown in Fig. 4 of Hiramoto at a lower cost. Thus, Hiramoto's Fig. 4 fails to disclose or suggest the Applicants invention. Although, Hiramoto's Fig. 7 shows the TSA function, the feature of Applicants claimed invention resides in that the TSA function is included in the high-speed interface circuit pack. Further, Hiramoto fails to disclose or suggest the Applicants invention in which the TSI function is also realized by replacing the connecting circuit pack interconnecting the high-speed interface pack and the low-speed interface circuit pack by the add/drop circuit pack. Accordingly, Hiramoto does not anticipate claims of the application and Applicants request withdrawal of the rejection thereof.

The Office Action rejects claims 1-2 under 35 U.S.C. § 102 over Takatsu (USP 5,311,501). This rejection is respectfully traversed.

Takatsu does not disclose or suggest that if the TSI function is not required, the circuit pack having the TSI function is replaced by the low-cost connecting circuit pack to reduce the manufacturing cost of the entire node. Accordingly, Takatsu does not anticipate claims of the application and Applicants request withdrawal of the rejection thereof.

For at least these reasons, it is submitted that the application is in condition for allowance. Prompt consideration and allowance are solicited.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

The Office is authorized to charge any fees due under 37 C.F.R. § 1.17 or 1.18 to Deposit Account No. 11-0600.

Should there be any questions concerning this matter, the Examiner is invited to contact Applicants' undersigned attorney.

Respectfully submitted,

Dated: February 24, 2003

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APPENDIX

VERSION SHOWING ADDED NEW CLAIMS 3 AND 4

IN THE CLAIMS:

Please add new claims 3-4 as follows:

3 (NEW) The multiplex conversion unit according to claim 1, wherein said multiplex conversion unit is applicable to one of Uni-directional Path Switched Ring (UPSR) and Terminal MUX (TM) networks by selectively combining said four types of circuit packs.

4. (NEW) The multiplex conversion unit according to claim 2, wherein said

multiplex conversion unit is applicable to one of 4-fiber Bi-directional Line Switched Ring (BLSR), 2-fiber BLSR and Linear ADM (LADM) networks by selectively combining said four types of circuit packs.